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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 19

Application Number: 09/085,298
Filing Date: May 27, 1998
Appellant(s): GOLDBERG, RICHARD TODD

Rodney M. Anderson
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the Remand to the Examiner from The Board of Patent Appeals and Interferences mailed on August 21, 2003.

The examiner is asked to further respond to the following argument as stated on page 3 of the Reply Brief: "[t]here's no teaching from the Nozaki et al. reference or from extrinsic evidence that the oxygen contaminant of the reference is present in sufficient amount, or at the appropriate time in the process, or even in a chemically combinable or active form, to cause oxidation of the underlying silicon surface. For example, referring to the disclosed Auger analysis in the reference, one can readily surmise that the amount of oxygen released from the quartz tube is insufficient to oxidize the silicon, or that the oxygen released from the quartz tube is produced too late in the process (i.e., after the silicon nitride is already formed) to reach and oxidize the silicon".

In response, the Examiner respectfully disagrees because the Appellant appears to be arguing about certain features which are not recited in the rejected claims. For example, Appellant argues that the Nozaki et al. reference fails to disclose providing sufficient amount of oxygen to oxidize the silicon-containing structure after the silicon nitride is formed. However, upon further inspection of the rejected claims, the Examiner has not been able to point out any limitation supporting such argument or any limitation relating to the time in the process when oxygen is released to reach and oxidize the silicon. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

But regardless, Nozaki et al. discloses at column 7, lines 9-12 that a high concentration of nitrogen and a low concentration of oxygen are already present at the surface of the silicon substrate prior to a thermal processing step to form a silicon nitride dielectric layer. Similar to the thermal processing step of the instant invention which requires a temperature range of at least

700°C (see Appellant's specification, page 7, lines 6-8), the thermal processing step of Nozaki et al. is carried out at approximately 800-1,300°C (see Nozaki et al., col. 7, lines 2-6). Therefore, because Nozaki et al. has shown the existence of oxygen and nitrogen prior to the thermal processing step, thermal nitridation and thermal oxidation of the silicon substrate must occur at the temperature range as shown. Nozaki et al. further discloses in TABLE 1 that oxygen in various concentrations are still present in the silicon nitride dielectric layer after the thermal processing.

The dielectric layer of Nozaki et al. appears to be an oxynitride or a nitrioxide. Support for the previous statement can be found on page 300, lines 6-9 of the text book, *Silicon Processing for the VLSI Era*, Volume 1 - Process Technology, Second Edition, Published 1986 (see attachment). According to Wolf et al., the authors of the book, a nitrided oxide ("oxynitride" or nitrioxide") layer is grown directly from N_2O or NO, or mixture of those gases with O_2. Wolf et al. further states that "when the oxide layer is grown this way, the nitrogen tends to be more uniformly distributed within the oxide". Therefore, Appellant's argument is wholly without merit because each claimed feature is clearly present in the Nozaki et al. reference.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Khanh Duong
March 5, 2004

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SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

Second Edition

STANLEY WOLF Ph.D.

RICHARD N. TAUBER Ph.D.

LATTICE PRESS

Sunset Beach, California

PREFACE
SECOND EDITION

This second edition of *Silicon Processing for the VLSI Era: Volume 1 - Process Technology* follows the 1986 publication of the first edition. More than 20,000 volumes of that version were sold, attesting to its widespread acceptance throughout the microelectronics community. Professionals and students of this vibrant technology should find the new edition equally useful.

Many new processes and materials have been incorporated into IC fabrication in the fifteen years since the first edition was written. The new materials and processes covered in the second edition include: 300-mm wafers, DUV lithography, chemically-amplified resists, high-energy ion implantation, high-density plasma sources for CVD and etching, step-and-scan aligners, chemical-mechanical polishing, dual-damascene interconnects, copper metallization, and low-*k* dielectrics. Altogether the material of our book comprises more than 900 pages, 600 illustrations, and 1500 references (with over half of the citations from 1996 to 1999). It also includes those topics from the first edition that are still in use.

The effort of writing and producing this new edition was predominantly carried out by Stanley Wolf. He revised eight chapters (Chaps. 1, 2, 3, 4, 6, 11, 12, and 14), and entirely wrote the five new ones (Chaps. 5, 13, 15, 16, and 17). Three chapters were revised by Richard N. Tauber (Chaps. 7, 8, and 9), and Michael Current revised Chap. 10.

Valuable input to Stanley Wolf was also provided by many persons. Foremost of these were R. N. Tauber and C. A. Wolf. They each carefully read the entire manuscript and offered extensive editorial assistance (Tauber: primarily technical, and Wolf: grammatical). Others who provided important technical assistance and critical reviews were: Jerry Healey, Richard Cohen, Chris Mack, Bruce Smith, Robert Simonton, Dennis Hess, Moshe Preil, Wilbur Krussell, Bob Climo, Kathleen Perry, Peter Lowenberg, and Donald Smith. Roy Montebin, of Vox Mundi, designed the book's cover.

Stanley Wolf, Ph.D.
Professor Emeritus, Department of Electrical engineering, CSULB

I would also like to acknowledge the support of my former colleagues at Applied Materials for their helpful discussions and for kindly providing some of the figures used herein: Chris Fulmer, Gary Miner, Gary Xing, Kelly Truman, Majeed Foad, Norma Riley, Parvin Katebi, and Satheesh Kuppurao.

In addition, I would like to thank the following persons for providing additional background material and figures used in this textbook: Al Geise - SVG/Thermco; Clyve Hayzelden - KLA/Tencor; Gerhardt Kneissal - ADE; Jim Cable - Peregrine Semiconductor; Pat Shanks - Semitool; Sang-Shin Kim - GaSonics; and Terry Ma - Avant!/TMA.

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relieve the stress in the film. Unfortunately, the thermal budget allowed for ULSI devices does not afford the luxury of high temperature processing.

8.9 THE OXIDATION OF SILICON NITRIDE

During the field oxide growth in the LOCOS isolation process (see Chap. 17), some oxide will form on the surface of the silicon nitride film. The oxide grows as a result of conversion of nitride to oxide. The conversion is a slow, self-limiting process. During field oxidation, when 400 nm of oxide grows on silicon, only 1–2 nm of oxide will grow on the nitride. But, the presence of the oxide can cause a process issue during the nitride strip step. If the nitride strip is done in hot phosphoric acid, it is necessary to first strip the thin oxide on the nitride in HF. Unless this oxide is removed, the phosphoric acid that etches the nitride will not remove the oxide, and stripping of the nitride will be retarded. If the nitride strip is done in a downstream plasma system, the problem is mitigated (since the oxide will etch in the CF_4 chemistry). However, the process must still include provisions for removing any oxide formed on the nitride.

8.10 THERMAL NITRIDATION OF SILICON AND SILICON DIOXIDE

Thermal nitridation (with ammonia) directly on silicon to produce silicon nitride was first aimed at generating a gate quality dielectric to replace silicon dioxide. The hope was that silicon nitride would have less defect density and higher breakdown strength than the oxide. These lofty goals were never achieved. As a matter of fact, devices made with directly nitrided gates have poor charge trapping and very high interface state densities. Thermal nitridation is achieved by reacting NH_3 with silicon according to:

$$3\ Si\ (solid) + 4\ NH_3\ (gas) \rightarrow Si_3N_4\ (solid) + 6\ H_2\ (gas) \qquad (8.35)$$

The growth of the nitride is extremely slow and self-limiting, since nitrogen cannot easily diffuse through the growing nitride film to react with silicon. (Silicon nitride is one of the best barriers to diffusion used in ULSI processing, see Chap. 6.) It is possible to grow only 3–4 nm of silicon nitride at high temperatures. There is a DRAM capacitor application where 1.5–2.0 nm of thermal nitride is grown on polysilicon at 900°C for 1 min using RTP. This nitride layer serves as a barrier to prevent further oxidation of the polysilicon during subsequent processing.

The nitridation of thermal oxides (the nitrided oxide film being called an *oxynitride* or even a *nitrioxide*), has resulted in improvements for thin gate oxides (<4 nm) and tunnel oxides (<10 nm). Some of the benefits realized include: a) improved resistance to boron penetration; b) increased V_{BD} and Q_{BD}; c) improved resistance to radiation damage; and d) improved endurance in flash memories. Some of the disadvantages reported for nitrided oxides include: a) increased fixed charge and interface state density and b) reduced channel mobility.

The techniques available for forming nitrided oxides are too numerous to discuss in detail here. This field is a very fertile area of research with new articles being published each month. Hence, only a brief number of the current techniques can be listed. Interested readers should consult the post-1995 journals and meetings publications of various technical societies for the latest work in this area. (Some of these include: *Applied Physics Letters*; *Electron Device Letters*; *Technical Digest of the IEDM*; the *Digest of the Papers of the VLSI Technology Symposium*; and the *Proceedings of the Spring Meetings of the Materials Research Society*).

There are two main ways to form a nitrided oxide. The first is to grow a silicon dioxide layer and then anneal that layer in either ammonia (NH_3), nitrous oxide (N_2O), or nitric oxide (NO).

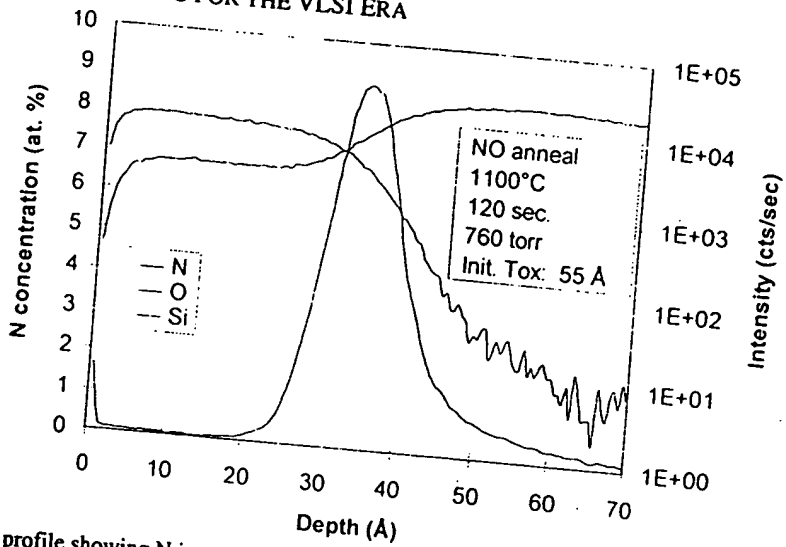

Fig. 8-22 SIMS profile showing N incorporation at the SiO_2 interface after annealing a thermal oxide in NO at 1100°C for 120 sec. Courtesy of Applied Materials.

The annealing is often performed in an RTP system, but a furnace can also be used. The annealing technique puts nitrogen into the oxide near the Si/SiO_2 interface. The nitrogen concentration and distribution can be measured using either SIMS or medium ion backscattering. Fig. 8-22 shows a SIMS plot of the nitrogen concentration for a NO annealed 3.3 nm oxide. The peak nitrogen concentration is 9% atomic, but the value depends on the temperature and time of the anneal. The second technique is to grow the oxide directly in N_2O or NO, or mixtures of those gases, with O_2. When the oxide is grown this way the nitrogen tends to be more uniformly distributed within the oxide. When using N_2O growth only about 1.5–2.0% nitrogen can be incorporated in the oxide.

8.11 TWO-DIMENSIONAL OXIDE-GROWTH EFFECTS

It is important to consider two-dimensional oxide growth when considering such effects as birds beak encroachment, oxide thinning, trench corner rounding, and gate bird's beak.

8.11.1 Birds Beak Encroachment

During the isolation process called *LOCal Oxidation of Silicon* (LOCOS), a thick oxide is grown in the field region of MOSFETs (while the active device region is protected by a masking layer of silicon nitride, see Chap. 16). Since oxidation can occur in two-dimensions, some oxidant diffuses under the edges of the nitride where unwanted oxide grows. The growth under nitride decreases as oxidant moves inward under the nitride edge. As a result, a gradually tapering oxide wedge merging into the pad oxide forms under the nitride. The oxide grown under the nitride can lift the nitride edges. The shape of the field oxide as it penetrates under the nitride has been given the name *bird's beak*. The bird's beak is a lateral extension of the field oxide into the active area of the device. Figure 8-23 shows an example of the bird's beak.[44] The length of the bird's beak depends on the thickness of the pad oxide and nitride layers, and on the oxidation temperature and pressure. The length of the bird's beak for a 500-nm thick field oxide is about 500 nm on a side. Thus, a lithographically defined active region of 1 μm will virtually disappear after field oxidation. To accommodate the bird's beak it is necessary to make the active region larger. This uses extra chip real estate and is inefficient for ULSI circuits.